CLAIMS

What is claimed is:

1. A computer system, comprising:

a control signal source;

a control signal destination;

a control signal path having a length, the control signal path coupling the control signal source and control signal destination, comprising:

a first plurality of signal paths each having two ends, a source end of a selected path of the first plurality of signal paths coupled to the control signal source;

a second plurality of signal paths each having two ends, a destination end of a selected path of the second plurality of signal paths coupled to the control signal destination;

a spanning circuit coupling the selected path of the first plurality of signal paths to the selected path of the second plurality of signal paths; and

wherein the length of the control signal path is at least a the sum of a length of the selected path of the first plurality of signal paths and a length the selected path of the second plurality of signal paths.

2. The computer system as defined in claim 1 wherein the spanning circuit further comprises:

a medial solder pad;

a first zero ohm resistor connecting a remaining end of the selected path of the first plurality of signal paths to the medial solder pad; and

a second zero ohm resistor connecting a remaining end of the selected path of the second plurality of signal paths to the medial solder pad.

3. The computer system as defined in claim 2 wherein the coupling between the control signal source and the source end of selected path of the first plurality of signal paths further comprises:

a source solder pad coupled to said control signal source;

a zero ohm resistor connecting the source solder pad to the source end of the selected path of the first plurality of signal paths.

4. The computer system as defined in claim 2 wherein the coupling between the control signal destination and the selected path of the second plurality of signal paths further comprises:

a destination solder pad coupled to said control signal destination;

a zero ohm resistor connecting the destination solder pad to the destination end of the selected path of the second plurality of signal paths.

5. The computer system as defined in claim 1 further comprising:

the control signal source is a clock source;

the control signal destination is a memory controller;

the control signal path is a clock signal path; and

wherein the memory controller uses a clock signal propagating on the clock signal path as a read clock for reading data from a memory bus.

6. The computer system as defined in claim 1further comprising:

the control signal source is a feedback output of a phased locked loop (PLL);

the control signal destination is a feedback input of the PLL; and

the control signal path is a feedback path of the PLL, and the length of the feedback path controls a phase relationship between an input signal to the PLL and an output signal of the PLL.

7. The computer system as defined in claim 1 wherein at least two of the first plurality of signal paths have different lengths.

8. The computer system as defined in claim 7 wherein at least two of the second plurality of signal paths have different lengths.

9. The computer system as defined in claim 1 wherein each of the first plurality of signal paths have different lengths.

10. The computer system as defined in claim 9 wherein each of the second plurality of signal paths have different lengths.

11. The computer system as defined in claim 10 wherein each of the first and second plurality of signal paths have different lengths.

12. The computer system as defined in claim 11 wherein lengths of each of the signal paths in the first and second plurality of signal paths are select so that each unique path through the control signal path has a unique length.

13. A method of adjusting timing of a control signal from a signal source to a signal destination, comprising:

coupling an adjustable signal path circuit having a plurality of possible signal path lengths between the signal source and the signal destination;

adjusting a length of a signal path through the adjustable signal path circuit to selectively add time delay to the control signal comprising:

selecting a first signal path in a first cluster of possible signal paths, said first signal path having a length;

selecting a second signal path in a second cluster of possible signal paths, said second signal path having a length;

coupling the first and second signal paths; and

forcing the control signal to propagate along the overall signal path having a length comprising the first and second signal paths.

14. The method as defined in claim 13 wherein said selecting the first and second signal paths further comprise:

coupling a source end of the first signal path to the control signal source using a zero ohm resistor;

coupling a second end of the first signal path to a second end of the second signal path using a zero ohm resistor; and

coupling a destination end of the second signal path to the control signal destination using a zero ohm resistor.

15. The method as defined in claim 14 wherein coupling the second end of the first signal path to a second end of the second signal path further comprises:

connecting the second end of the first signal path to a medial solder pad using a zero ohm resistor; and

connecting the second end of the second signal path to the medial solder pad using a zero ohm resistor.

16. The method as defined in claim 15 wherein coupling a source end of the first signal path to the control signal source further comprises:

coupling the control signal source to a source contact pad; and

connecting the source end of the first signal path to the source contact pad by way of a zero ohm resistor.

17. The method as defined in claim 15 wherein coupling a destination end of the second signal path to the control signal destination further comprises:

coupling the control signal destination to a destination contact pad;

connecting the destination end of the second signal path to the destination pad by way of a zero ohm resistor.

18. The method as defined in claim 13 further comprising:

selecting a unique length for each of the first cluster of possible signal paths;

selecting a unique length for each of the second cluster of possible signal paths; and

selecting said unique lengths for the first and second clusters of possible signal paths such that each combination of the first and second signal paths have unique lengths.

19. A computer system comprising:

a control signal source;

a control signal destination;

a control signal path having a length, the control signal path coupling the control signal source and control signal destination, comprising:

a first plurality of signal paths, a source end of a selected first path of the first plurality of signal paths coupled to the control signal source;

a second plurality of signal paths, a destination end of a selected second path of the second plurality of signal paths coupled to the control signal destination;

a third plurality of signal paths;

a first spanning circuit coupling the selected first path to a selected third path of the of the third plurality of signal paths; and

a second spanning circuit coupling the selected third path to the selected second path;

wherein the length of the control signal path is at least the sum of a length of the selected first path, a length the selected second path, and a length of the selected third path.

20. The computer system as defined in claim 19 wherein the first spanning circuit further comprises:

a first solder pad;

a first zero ohm resistor connecting the first solder pad to the selected first path; and

a second zero ohm resistor connecting the first solder pad to the selected third path.

21. The computer system as defined in claim 19 wherein the second spanning circuit further comprises:

a first solder pad;

a first zero ohm resistor connecting the first solder pad to the selected third path; and

a second zero ohm resistor connecting the first solder pad to the selected second path.

22. The computer system as defined in claim 19 further comprising:

the control signal source is a clock source;

the control signal destination is a memory controller;

the control signal path is a clock signal path; and

wherein the memory controller uses a clock signal propagating on the clock signal path as a read clock for reading data from a memory bus.

23. The computer system as defined in claim 19 further comprising:

the control signal source is a feedback output of a phased locked loop (PLL);

the control signal destination is a feedback input of the PLL; and

the control signal path is a feedback path of the PLL, and the length of the feedback path controls a phase relationship between an input signal to the PLL and an output signal of the PLL.

24. The computer system as defined in claim 19 wherein only one source end of the first plurality of signal paths couples to the control signal destination.

25. The computer system as defined in claim 19 wherein only one destination end of the second plurality of signal paths couples to the control signal destination.

26. A computer system having a control signal between a first and second device, comprising:

a solder pad coupled to said first device;

a first signal path having a length;

a zero ohm resistor connecting said solder pad to said first signal path;

a second solder pad;

a second zero ohm resistor connecting said first signal path to said second solder pad;

a second signal path having a length;

a third zero ohm resistor connecting the second solder pad to said second signal path;

a third solder pad;

a fourth zero ohm resistor connecting the second signal path to the third solder pad;

where said third solder pad coupled to said second device;

a first plurality of unused signal paths spanning the first and second solder pads, but not electrically connecting those pads; and

a second plurality of unused signal paths spanning the second and third solder pads, but not electrically connecting those pads;

wherein said first device drives a control signal across said first and second signal paths, and wherein said second device reads said control signal; and

wherein the time required for said control signal to propagate between the first and second devices is proportional to a length traveled between the two devices comprising the length of the first and second signal paths.

27. A computer system, comprising:

a microprocessor coupled to a primary bridge device;

a main memory array coupled to a memory controller by way of a memory bus, said memory controller integral with said primary bridge device;

a secondary bridge device coupled to said primary bridge device by way of a primary expansion bus;

an input/output controller coupled to said secondary bridge device by way of a secondary expansion bus;

a keyboard coupled to said input/output controller;

an adjustable signal delay circuit coupled between a control signal source and a control signal destination, said adjustable signal delay circuit time delays a control signal, said adjustable time delay circuit comprising:

a first plurality of signal paths each having two ends, a source end of a selected path of the first plurality of signal paths coupled to the control signal source;

a second plurality of signal paths each having two ends, a destination end of a selected path of the second plurality of signal paths coupled to the control signal destination;

a spanning circuit coupling the selected path of the first plurality of signal paths to the selected path of the second plurality of signal paths; and

wherein the length of a control signal path through the adjustable time delay circuit is at least a the sum of a length of the selected path of the first plurality of signal paths and a length the selected path of the second plurality of signal paths.

28. The computer system as defined in claim 27 wherein the spanning circuit further comprises:

a medial solder pad;

a first zero ohm resistor connecting a remaining end of the selected path of the first plurality of signal paths to the medial solder pad; and

a second zero ohm resistor connecting a remaining end of the selected path of the second plurality of signal paths to the medial solder pad.

29. The computer system as defined in claim 28 wherein the coupling between the control signal source and the source end of selected path of the first plurality of signal paths further comprises:

a source solder pad coupled to said control signal source;

a zero ohm resistor connecting the source solder pad to the source end of the selected path of the first plurality of signal paths.

30. The computer system as defined in claim 28 wherein the coupling between the control signal destination and the selected path of the second plurality of signal paths further comprises:

a destination solder pad coupled to said control signal destination;

a zero ohm resistor connecting the destination solder pad to the destination end of the selected path of the second plurality of signal paths.

31. The computer system as defined in claim 27 further comprising:

the control signal source is a clock source;

the control signal destination is the memory controller;

the control signal path is a clock signal path; and

wherein the memory controller uses a clock signal propagating on the clock signal path as a read clock for reading data from the memory bus.

32. The computer system as defined in claim 27 further comprising:

the control signal source is a feedback output of a phased locked loop (PLL);

the control signal destination is a feedback input of the PLL; and

the control signal path is a feedback path of the PLL, and the length of the feedback path controls a phase relationship between an input signal to the PLL and an output signal of the PLL.